Uplink Performance Evaluation of Packet Combining ARQ for MPR Prefix-Assisted DS-CDMA

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Abstract—Prefix-assisted direct-sequence code-division multiple access (DS-CDMA) is a viable transmission technique for high-data-rate wireless broadband systems, capable of coping with highly dispersive channels at the uplink. Packet combining (PC) ARQ with an iterative block decision feedback equalization (IB-DFE) technique can be used to cope with errors. However, extracting the IB-DFE's packet error rate (PER) for MAC-layer simulations can be time consuming. Most works that model the DS-CDMA behavior with PC ARQ use simplified asymptotic PER models in the study of the system performance, which are not precise for low signal-to-noise ratios and for a low number of mobile terminals (MTs). In this paper, the MAC performance is modeled using a discrete-time Markov chain that relies on a PER model. As an example, this paper describes a PER analytical model for an uncoded prefix-assisted DS-CDMA system with PC ARQ that considers the following inputs: the number of MTs accessing the channel, the MTs' number of transmissions, and the channel realizations for a given bit energy over noise ratio. The results show that the model portrays with better accuracy the simulations' results, compared with an alternative asymptotic model.

Index Terms—Packet combining ARQ, prefix-assisted DS-CDMA, IB-DFE, DTMC, analytical model.

I. INTRODUCTION

PREFIX-assisted Direct Sequence Code Division Multiple Access (DS-CDMA) [1] is a viable transmission technique for high data-rate wireless broadband systems, capable of coping with highly dispersive channels at the uplink. DS-CDMA can multiplex several Mobile Terminals (MTs) at the uplink

channel, by assuming all MTs use unique orthogonal spreading codes, which is referred to as CDMA's Multi-Packet Reception (MPR) ability [2]. Wireless CDMA packet-data-oriented systems have been a hot research topic in the last decades, attracting contributions regarding the design and analysis of the performance of physical (PHY) layer receiver algorithms (focused on minimizing the Packet Error Rate (PER), e.g., [2]–[4]) or the system-level throughput performance (which depends on the logical-layer protocols, including the Medium Access Control (MAC) and Automatic Repeat-reQuest (ARQ) protocols, e.g., [5]). A small number covers a quantitative understanding of the joint effects on the throughput performance of the PHY and MAC layers (e.g., [6], [7]). However, they usually considered approximated PHY layer asymptotic models that loose precision for a low signal-to-noise ratio (SNR) and for a low number of MTs.

Packet Combining (PC) ARQ is a common solution to handle a low SNR scenario: the receiver may store failed packet copies (due to high noise or interference levels) and combine them to retrieve the data symbols. PC ARQ [8] takes advantage of the time diversity from each packet transmission requested by the receiver to retrieve the packets' data symbols. If the receiver is unable to retrieve the received data packets with success, due to a deep-fade that persists for several slots in the wireless channel, the receiver can improve data reception through FDE techniques [4]. With the aid of a non-linear iterative equalization method such as Iterative Block with Decision Feedback Equalization (IB-DFE) [9], the receiver can diminish high channel interference or residual interference between MTs to enhance data reception, similar to Successive Interference Cancellation (SIC).

The performance of a prefix-assisted DS-CDMA system with PC at the uplink depends on the channel effects and on the interference measured at the receiver. Interference is defined by the number and power distribution of the MTs transmitting in each of the slots where a given packet is transmitted [10], but also on how much residual interference was not removed at the receiver. A common approach is to define a minimum SINR threshold value above which the receiver satisfies the Quality of Service (QoS) requirements. Approximated values are calculated for the receiver's Bit Error Rate (BER) (e.g., [7], [11]–[13]), using average interference estimations that consider the receiver's asymptotic performance when the number of users and the spreading gain tend to infinity and their ratio converges to a constant. Until now, most of the authors assumed that the number of MTs transmitting during the PC ARQ transmissions

remained constant for an average number of colliding MTs. Bigloo *et al.* [14] assumed that the composite packet arrivals (including both new arrivals and retransmissions) in different slots are independent and identically Poisson. Multidimensional Markov chain models were used for the system dynamics in [7], [15]. The average BER is obtained from steady-state probabilities by solving a fixed-point equation [15] or applying the renewal-reward theorem [7], considering a simplified MAC-layer system state that accounts an estimation of the number of interfering MTs during all the packet transmissions. On the other hand, Levorato and Zorzi considered a comprehensive system model for the performance of CDMA with coded PC ARQ [6] regarding spatially distributed interfering signals in an ad hoc network. It describes the distribution of the number of packets decoded at a given stage using an embedded chain of a semi-Markov process in function of the node's distribution and error probability. However, the steady-state distributions for the interference and throughput are obtained using a recursive algorithm, where the SINR is approximated using the asymptotic model defined in [13]. So the PER considered is not precise for low SNR and for a low number of MTs, where more precise PHY layer models would be required.

Precise PHY-layer BER models were proposed for static interference patterns (e.g., considering a constant number of interfering MTs [3], [16]–[19]), usually requiring extensive Monte Carlo simulations to obtain the BER performance, or using *a priori* PER results that are time-consuming to extract. These precise PHY-layer models can only be applied if the MAC-layer system model describes all the relevant system level parameters, including the probability of occurring each interference pattern. This information is not provided by the existing system models, although it brings a higher overhead to the model due to the extended state space required. The potential gain is the possibility of modeling DS-CDMA systems that employ a lower transmission power (not covered by the asymptotic models), which may be more energy efficient.

In the authors' perspective this work distinguishes itself from existing works in the literature because the model proposed combines precise PHY-layer and MAC-layer models to improve the accuracy of the measured system level performance. Its main contributions are:

- A Discrete-Time Markov Chain (DTMC) wireless access model is proposed for the MAC-layer using the PHY-layer performance model, to estimate the statistics of the interference pattern;
- A performance model is proposed for the system's throughput, delay and expended Energy per Useful Packet (EPUP) for a uniform average load, calculated using the DTMC's steady state;

This DTMC model can be used to implement user admission, traffic throttling and other optimization decision processes using Markov Decision Processes approaches [20]. Furthermore, the analytical PHY-layer model in [21] is extended to cover a uncoded CDMA system using the IB-DFE PC technique considered. This PHY-layer model is used in a set of simulations, and the performance model proposed is compared with the one at [7].

The PER estimation considers both the receiver performance and the interference pattern statistics, and is capable of analyzing limit conditions with low SNR. The trade-off is the increased complexity that results from the enlarged system state considered.

The paper is structured as follows: the current section presented the related work and identified the contributions; Section II characterizes the DS-CDMA PC system; Section III describes the DTMC wireless access model; Section IV presents the IB-DFE receiver's PER calculation; Section V shows the proposed model results; and Section VI briefs the paper's conclusions.

II. SYSTEM DESCRIPTION

The proposed work assumes an infrastructured wireless system, with full-duplex communication, where a Base Station (BS) coordinates the wireless uplink access in a time slotted manner; MTs only access the channel when they have packets in their buffer to transmit or need to re-transmit a packet that was previously received with errors at the BS. For the sake of simplicity, perfect synchronization is assumed with time advance mechanisms; for a prefix-assisted DS-CDMA system, timing errors can be absorbed by the cyclic prefix since the cyclic prefix is longer than a symbol's duration, assuming that channel estimates are accurate enough.

The paper also assumes that a MPR PC receiver is used and that it is possible to calculate the PER for any given interference pattern, either using a physical layer analytical model or Monte Carlo simulations.

For a DS-CDMA spreading factor of K, each uplink slot should support up to K simultaneous transmissions, assuming that the wireless medium has $Q \leq K$ MTs contending the channel. It is also assumed that a data packet at the uplink has the same size of an uplink slot and that the BS is capable of detecting the number of MTs transmitting in an uplink slot.

Fig. 1 displays the frame structure of each slot, composed by a SYNC signal at the downlink and data symbols with their respective cyclic prefix at the uplink. The SYNC signal transmitted at the beginning of each slot by the BS, signals the start of each slot, so that all MTs associated with the BS know when to transmit in a synchronous way. The SYNC signal also indicates which packets were successfully received in the previous slot and requests retransmissions from packets that were received with errors. A packet at the head of the MT's buffer will be sent at the following slot with M modulated symbols. A MT with an empty queue will remain silent until a packet arrives at its queue. At the end of the slot the BS runs the reception algorithm, acknowledging at the beginning of the next slot all packets that were successfully received; packets with errors are retransmitted in the following slot and the signals from all copies received can be combined to improve the reception. A packet transmitted $(R + 1)$ times that is decoded with errors will be discarded from the MT's queue.

Each MT transmits packets independently. The BS uses a PC MPR receiver that holds information from previously received packets with decoding errors and their respective transmissions, and combines it with the signals received in the last slot. The
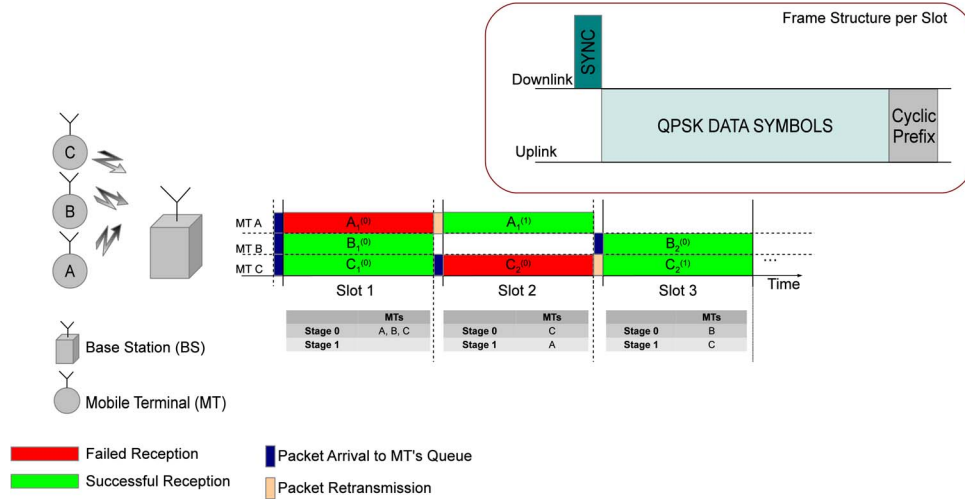
Fig. 1. PC ARQ prefix-assisted DS-CDMA Reception scheme example and frame structure per slot.

BS keeps track of how many retransmissions per MT have occurred, assuming that each transmission has a duration of one time slot. The BS groups MTs with the same number of transmissions per packet. If (some or) all of the MTs for a given number of retransmissions fail to transmit their packets then the BS will assign those MTs to the following retransmission group. If MTs succeed transmitting their packets then the BS removes them from the retransmission groups.

It is also assumed that the BS can store up to $(R + 1)$ failed transmissions from all MTs, keeping track of which MTs are on the lth retransmission, where $0 \leq l \leq R$; $l = 0$ represents the MTs with only one transmission. If a MT succeeds transmitting or transmits $R + 1$ times a data packet, then all of its transmissions are removed from the BS.

Fig. 1 presents a brief example of the modeled system, where three MTs A, B and C transmit data packets to a BS, assuming a retransmission limit of $R = 1$. In the scope of this paragraph, a packet from MT A for instance, is denoted in the figure as $A_i^{(r)}$, where $i = \{1, 2, \ldots\}$ denotes A's packet identifier and $r = \{0, 1, 2, \ldots, R\}$ the rth transmission. At the beginning of each slot the BS acknowledges the packets that were successfully received, with a SYNC block, and signals MTs the beginning of that same slot. At the first slot, the three MTs transmit data to the BS, where B's and C's packets are received by the BS with success, while A's packet, $A_1^{(0)}$, has errors. To recover from $A_1^{(0)}$'s errors, BS forces MT A to retransmit the same packet now denoted as $A_1^{(1)}$, and the BS will henceforth combine both $A_1^{(0)}$ and $A_1^{(1)}$ using the PC technique. During the second slot, MT C also transmits a second packet, $C_2^{(0)}$, though received with errors; in similar fashion, MT C will retransmit the same packet, denoted as $C_2^{(1)}$, at the same time as $B_2^{(0)}$. Both $C_2^{(1)}$ and $B_2^{(0)}$ are received with success.

III. DTMC ACCESS MODEL

The current section describes the Discrete-Time Markov Chain (DTMC) model, based on the assumptions of Section II. MTs transmit data according to a *Poisson* distribution with rate λ. In order to reduce the state space dimension, it is also assumed that the signal from all MTs is received with equal average power. Therefore, the DTMC state does not need to store who is transmitting, but only how many MTs are transmitting in each retransmission stage.

A. Steady-State Probability Distribution

The system state for a given slot, $\chi \in \Omega$, is defined by a collection of random values

$$\chi = \{\chi_e, \chi_0, \chi_1, \ldots, \chi_R\}; \tag{1}$$

χ_e stands for the random variable of the number of idle MTs and χ_l, $l \in [0, R]$, for the random variable of the number of MTs in the lth ARQ retransmission. The state space of χ is defined by the values $\vartheta = \{I, \vartheta_0, \vartheta_1, \ldots, \vartheta_R\}$, where I and ϑ_l, $l \in [0, R]$, are respectively the values of the number of idle MTs (χ_e) and the number of transmitting MTs at the lth retransmission (χ_l); these values are conditioned by the number of MTs that are associated with the BS, Q, where $I + \sum_{l=0}^{R} \vartheta_l = Q$. ϑ_0 denotes the number of MTs that have transmitted a packet once, i.e., without retransmissions (χ_0). So, the universe of system states can be described by (2), shown at the bottom of the page.

As an example, a state with Q idle MTs can be described as $\vartheta = \{I = Q, \vartheta_0 = 0, \ldots, \vartheta_R = 0\}$. From the aforementioned ϑ state, if n MTs out of Q have a packet to transmit, then χ will be described as $\vartheta = \{I = Q - n, \vartheta_0 = n, \vartheta_1 = 0, \ldots, \vartheta_R = 0\}$. The new system state can fork to several others, where

$$\Omega = \left\{ \chi_e = I, \chi_0 = \vartheta_0, \chi_1 = \vartheta_1, \ldots, \chi_R = \vartheta_R; \left(\{I, \vartheta_l\} \in \mathbb{N}_{[0,Q]}, l \in [0, R], I + \sum_{l=0}^{R} \vartheta_l = Q \right) \right\} \tag{2}$$